Remarks

Claims 1-20, and 22-35 remain in the application. Claims 1, 6, 8-10, 16, 18, 19, 22, 24, 26-29, 31 and 35 have been amended. Claim 21 has been cancelled.

Claim Rejections—35 USC 112

Regarding claim 1, Examiner has pointed out applicant's teaching as implying pipeline storage locations within a pipeline. Examiner has also stated that Examiner would interpret the term "pipeline" as pipeline storage location. Applicant has amended claim 1 of the invention to clearly distinguish between the invention, which comprises a pipeline, and which said pipeline further comprises storage locations in each stage of a pipeline or pipelines, as the case may be, which examiner is interpreting as being pipeline storage locations. Claim 1 stands amended, and Applicant believes, is now in order of acceptance. Hence, a request for allowance of claim 1 is hereby made.

The term "pipeline" used in claims 6, 8-10, 16, 18, 19, 21, 24, 26, 27-29, 31 and 35 has also been amended to read "pipeline storage locations" in each stage of a pipeline or pipelines, as the case may be.

Examiner rejected claims 1-28 under 35 USC 112, second paragraph as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. Claims 1 and 19 have been amended to include the alleged omitted steps of monitoring and controlling instruction dependency for microprocessors/microprocessor systems. Claims 1, 6, 8-10, 16, 18, 19, 21, 24, 26, 27-29, 31 and 35 have been amended as per Examiner's recommendations, and now, Applicant believes, meet the requirements

of 35 USC 112. Consequently, and in light of the above, a request for allowance of claims 1-20, and 22-35 is hereby made.

Claim Rejections—35 USC 101

Examiner rejected claims 1, 2, 11, and 19 under 35 USC 101 as being directed to non-statutory subject matter.

Regarding claim 1, claim 1 has been rejected for failing to provide a useful, concrete, and tangible result related to monitoring and controlling instruction dependency for microprocessors as indicated in the preamble. Claim 1 has been amended to include the step of "prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle" if there is a match. Thus, monitoring and controlling instruction dependency has been addressed without introducing any new matter, as the amended claim draws from the existing specification. Consequently, in light of the above, Applicant believes that claim 1 as amended is now in order of acceptance and respectfully requests that a 101 rejection be withdrawn and a notice of allowance be made.

Regarding claims 2 and 11, claims 2 and 11 are dependent upon claim 1, and as shown above, claim 1 is now in order of acceptance. Consequently, claims 2 and 11 are also in order of acceptance. Applicant thus respectfully requests that a 101 rejection to claims 2 and 11 be withdrawn and a notice of allowance be made.

Regarding claim 19, claim 19 has been rejected for failing to provide a useful, concrete and tangible result in all situations except when both statements e (amended,

now f) and e2 (amended, now f2) are true. Claim 19 has been amended to include a useful, concrete and tangible result even when statements e (now f) and e2 (now f2) are false, namely "if the destination operand of the instruction is not a temporary register: writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations." Claim 19 has been amended, with amendments incorporated from the specification as it exists, and includes no new matter. Applicant believes that claim 19, as amended, now provides a useful, concrete and tangible result related to monitoring and controlling instruction dependency for microprocessor systems as indicated in the preamble. Therefore, Applicant respectfully requests that a 101 rejection to claim 19, as amended, be withdrawn and a notice of allowance be made.

Claim Rejections—35 USC 102

Examiner rejected claims 1-35 under 35 USC 102(e) as being anticipated by Arnold et al. US Pat. No. 6,438,681, herein referred to as Arnold.

Regarding claim 1, Applicant's claim 1, as amended teaches "A method of monitoring and controlling instruction dependency for microprocessors, the method comprising: fetching an instruction at a thread control element; comparing one or more source operand identifications of the instruction to one or more temporary register identifications, wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations; [[and]] verifying whether any of the one or more source operand identifications matches any of the one or

more temporary register identifications[[.]]; in response to a match, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle, wherein the match corresponds to instruction dependency."

Clearly claim 1, as amended, of Applicant's teaching discloses a comparing and instruction execution stalling step that takes place outside the pipeline, and occurs between the arbiter, comparator and thread control elements. The cited reference on the other hand discloses register identifiers, in the pipeline stages, which register identifiers are referred to as consumers and producers. The instructions are described as being both consumers and producers (col. 5, lines 25-31) in that they both retrieve and store data during execution. The register identifier referred to as "producer" identifies a register wherein the instruction stores data even though the instruction may retrieve data from another register. The register identifier of an instruction referred to as consumer identifies a register where the instruction retrieves data even though the instruction may store data in another register, and therefore be associated with another register identifier. Determining whether a data dependency or data dependency hazard exists, takes place in the pipeline itself. An earlier stage of the pipeline or pipelines is compared with later stage/stages of the pipeline or pipelines to check if data dependency hazards exist or not.

In contrast, Claim 1 of applicant's teaching discloses a comparison between source operands in the thread control elements (TC0, TC1, and TC2) and one or more temporary register identifications stored in one or more temporary register identification pipelines (or pipeline storage locations), respectively. The cited reference, on the other hand, teaches of comparison between a register identifier (consumer) in one stage of a pipeline or pipelines with register identifiers (producer) in later stages of a pipeline or

pipelines. The comparator here takes one stage of the pipeline and compares it with other stages of the same pipeline to determine a data dependency hazard. In applicant's teaching, the comparator is comparing the source operand in the **thread control element** with a pipeline storage location in a pipeline and moving data forward to a next storage location in a pipeline, accordingly. Thus, the same thread control elements may be used with several pipelines, and complicated circuitry is reduced this way. Therefore applicant's claim 1 is not anticipated by the cited reference. Consequently, and in light of the above, applicant respectfully requests that a 102(e) rejection to claim 1 be withdrawn and a notice of allowance be made.

Regarding claims 2-18, claims 2-18 are dependent upon claim 1, and as shown above, Applicant's claim 1 is not anticipated by the cited reference of Arnold. Therefore claims 2-18 are not anticipated by Arnold. Consequently, and in light of the above, Applicant requests that a 102(e) rejection to claims 2-18 be withdrawn and a notice of allowance be made.

Regarding claim 19, examiner has rejected claim 19 as being anticipated by Arnold. In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. The cited reference at no point teaches comparison between a thread control element outside of a pipeline stage or storage location with each temporary register identification in the pipeline storage location of a pipeline. Rather the cited reference teaches of a comparator that compares a "consumer" in the pipeline with various "producers" in the same pipeline, and checks for data dependency. Note that in applicant's teaching, both the thread control element which fetches an instruction from

the arbiter and the arbiter are not part of the pipeline. The comparator in applicant's teaching is comparing an instruction in the thread control element with each temporary register identification in the pipeline storage locations. Applicant's teaching clearly indicates both in the specification and the drawings, that the thread control elements and arbiter are not part of the pipeline or pipeline storage locations. Thus, applicant's claim 19 is not anticipated by the cited reference. Consequently, in light of the above, Applicant respectfully requests that a 102(e) rejection to claim 19 be withdrawn and a notice of allowance be made.

Regarding claims 20-28, claim 20 and claims 22-28 are dependent upon claim 19, and as shown above, Applicant's claim 19 has not been anticipated by the cited reference of Arnold. Therefore, claims 20 and claims 22-28 are not anticipated by Arnold. Consequently, Applicant respectfully requests that a 102(e) rejection to claim 20 and claims 22-28 be withdrawn and a notice of allowance be made.

Claim 21 has been cancelled.

Regarding claim 29, examiner has rejected claim 29 as being anticipated by Arnold. In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. Examiner is in error. The cited reference only teaches of comparison between the n bit register identifier of one stage of the pipeline with the register identifiers of the other stages of the same pipeline. In contrast, Applicant's claim 29 teaches of comparing elements coupled to both thread control elements and to the temporary register identifiers of the pipeline in the pipeline storage locations. Examiner would kindly appreciate that the thread control elements are not part of the pipeline, but the instruction held in the

thread control element is compared with the temporary register identifier of the pipeline storage location in the pipeline for data dependency. Clearly, since the thread control element is not part of a particular pipeline, the instruction may be compared with temporary register identifiers of several pipelines. This reduces complicated circuitry, and is in fact an innovation over prior art. Consequently, and in light of the above, Applicant's claim 29 is not anticipated by the cited reference of Arnold. Therefore, Applicant respectfully requests a 102(e) rejection to claim 29 be withdrawn and a notice of allowance be made.

Regarding claims 30-34, claims 30-34 are dependent upon claim 29 and as shown above, claim 29 is not anticipated by the cited reference of Arnold. Therefore, claims 30-34 are not anticipated by Arnold. Consequently, Applicant respectfully requests that a 102(e) rejection to claims 30-34 be withdrawn and a notice of allowance be made.

Regarding claim 35, examiner has rejected claim 35 as being anticipated by Arnold. In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. The cited reference only teaches of comparison logic that determines whether a data dependency exists or if there is a data dependency hazard. Applicant's claim 35, on the other hand, teaches of a system for not just instruction dependency monitor, but control as well. Examiner is in error, since the cited reference does not anywhere disclose an arbiter coupled to thread control elements, comparing elements, and the temporary register pipelines. Support is found for Applicant's claim 35 wherein in the specification it is recited that "the arbiter **107** receives a match alert from a comparator, the arbiter prohibits the instruction held in the corresponding thread control element from

executing in that clock cycle." (Page 9, lines 4-6). Examiner tries to draw an analogy between the instruction dispersal unit of the cited reference and the arbiter of Applicant's claim 35. Applicant humbly submits that such an analogy is misplaced. Applicant's claim 35 clearly teaches of an arbiter coupled to the thread control elements, comparing elements, and the temporary register pipelines. Neither figure 1 nor figure 3 of the cited reference show the instruction dispersal unit coupled to the comparison logic. Further, the cited text also does not teach of the instruction dispersal unit either monitoring or controlling instruction dependency. The comparison logic of the cited reference is used to compare the "consumer" with each of the "producer" identifiers for data dependency. Consequently, and in light of the above, Applicant's claim 35 is not anticipated by the cited reference. Therefore, Applicant respectfully requests that a 102(e) rejection to claim 35 be withdrawn and a notice of allowance be made.

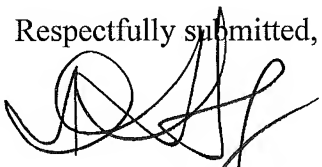
CONCLUSION

In view of the foregoing, the Applicant believes that all of the claims are now in condition for allowance and respectfully request the Examiner to issue a timely Notice of Allowance in this case. If for any reason, the Examiner believes any of the claims are not in condition for allowance, he is encouraged to call the undersigned attorney at 650-325-4999 so that any remaining issues may be resolved.

The above changes are believed not to add new matter, as support is found in the specification as described above.

Claims 1-20, and 22-35 remain in this application. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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